iATC 2952
INTEGRATED LINE CARD CONTROLLER

- **Provides Complete Backplane Interface for 8 Subscribers**
- **Performs all Timeslot Assignments**
- **2 Full-Duplex, Serial TDM Highways**
- **Serial, Bidirectional Packetized highway for Signaling Control**
- **Standard MCS μP interface with two channel DMA and interrupt**
- **Implements HDLC Protocol to Guarantee Integrity of all Signaling and Control Information**
- **Supports Four Control Options Local or Global Microprocessor Direct or Interleaved HDLC Control**
- **Designed for 24, 32, 48 or 64 Timeslot Systems**
- **Common Backplane Interface Supports ISDN Upgradability**

The Intel iATC 2952 Line Card Controller (LCC) is a special purpose I/O controller optimized for use in all types of telecommunication switching systems. The 2952 is intended for use with up to eight subscriber devices in both analog and digital line circuits. It is also useful as a general purpose I/O controller for other applications.

The 2952 represents the continuation of a trend to intelligent flexible line cards. With its modular design, the 2952 provides a graceful upgrade path from analog line circuits to an all digital system. Analog line board density can be greatly increased using the LCC with the 29C51 Feature Control Combo. The 2952 handles the transfer of primary voice, data, feature control, and signaling information between the backplane and up to 8 29C51's. The 2952 emphasizes highly serial interfaces, thus reducing the number of digital interconnections both to the subscriber device and to the backplane.

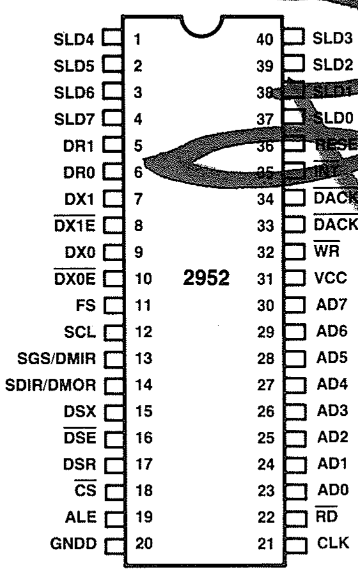

Figure 1. Pin Configuration

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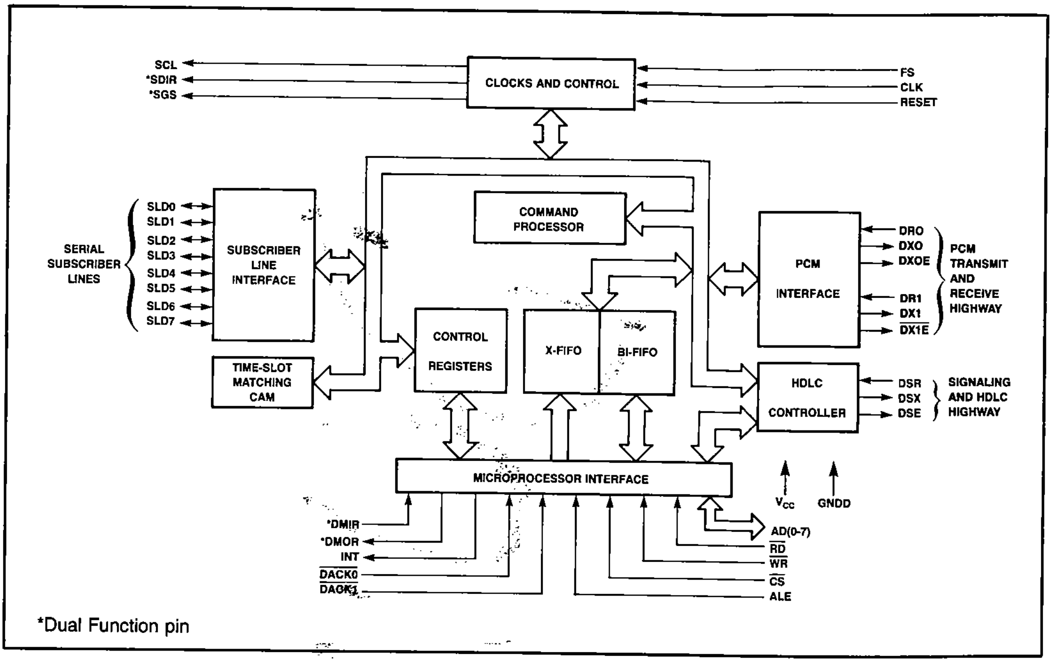


Figure 2. 2952 Block Diagram

Table 1. Pin Description

Symbol	Pin No.	Function
GNDD	20	Ground: OV.
VCC	31	Most positive supply; input voltage is +5V ±5%.
SLD0–7	37–40 1–4	Subscriber Data Link. There are eight bidirectional pins that transfer serial information between the 2952 and the subscriber devices (e.g. 29C51).
SCL	12	Subscriber Clock. This is a 512kHz signal generated by the 2952 with 50% or 33% duty cycle clock. Can be connected up to 8 slave devices.
SGS/DMIR	13	Signaling Strobe. Can be used to strobe signaling bits or voice bytes for enabling external logic. In the DMA mode DMIR functions as DMA input request for HDLC.
SDIR/ DMOR	14	Subscriber Direction. This is an 8kHz signal generated by the 2952 to serve as both a direction indicator and a slave frame sync. When high, the SLD bus becomes an output and data is transferred from the 2952 to the slave. When low, the output buffer on the slave SLD pin is enabled and data is transferred from the slave to the 2952. In the DMA mode, DMOR functions as DMA output request for HDLC.
$\overline{CS}$	18	Chip Select. Enables $\overline{RD}$ or WR. A low level at this input allows the 2952 to accept commands or data from a microprocessor within a write cycle, or to transmit data during a read cycle. When no local uP is connected this pin should be connected to GNDD.
ALE	19	Address Latch Enable. (Active high input). On falling edge of this input signal, data on AD(0–7) is latched into the selected register. When no local microprocessor is connected, this pin should be connected to GNDD.
$\overline{RD}$	22	Read Strobe. (Active low input). When input is low, data is transferred from selected register on to μP bus. When no local μP is connected, this pin should be connected to GNDD.
AD(0–7)	23–30	Address/Data pins. Standard μP bus used to transfer address and data between the μP and internal registers of the 2952. When no local μP is connected, the unique ID is hardwired on pins AD(0–7).
$\overline{WR}$	32	Write Strobe. (Active low input). When $\overline{WR}$ transitions from low to high, data on pins AD(0–7) are latched into the selected register. When no local microprocessor is connected, this pin should be connected to GNDD.
$\overline{DACK0}$ $\overline{DACK1}$	33 34	DMA Acknowledge. $\overline{DACK0}$ is used to acknowledge the DMA output, and $\overline{DACK1}$ is used for DMA input. When no local microprocessor is connected, these pins are used to hardwire mode information.
$\overline{INT}$	35	Interrupt Request. A standard microprocessor interrupt, with active low output.
DR1	5	Receive PCM Highway 1. Serial words are received on PCM highway 1 at this interface.
DR0	6	Receive PCM Highway 0. Serial words are received on PCM highway 0 at this interface.
DX1	7	Transmit PCM Highway 1. Serial words are transmitted onto PCM highway 1 at this interface.
$\overline{DX1E}$	8	Transmit PCM Highway 1 Enable. Used to enable external tristate buffers to drive signals onto the PCM highway. The signal goes low while the 2952 is transmitting onto PCM highway 1.

Table 1. Pin Description

Symbol	Pin No.	Function
DX0	9	Transmit PCM Highway 0. Serial words are transmitted onto PCM highway 0 at this interface.
$\overline{\text{DX0E}}$	10	Transmit PCM Highway 0 Enable. Used to enable external tristate buffers to drive signals onto the PCM highway. The signal goes low while the 2952 is transmitting onto PCM highway 0.
DSX	15	Transmit Signaling Highway. Serial signaling and control data is transmitted on this dedicated HDLC highway.
$\overline{\text{DSE}}$	16	Transmit Signaling Highway Enable. Used to enable external tristate buffers to drive signals onto the transmit signaling highway. The signal goes low while the 2952 is transmitting an HDLC packet onto DSX.
DSR	17	Receive Signaling Highway. Serial signaling and control data is received on this dedicated HDLC highway.
FS	11	Frame Synchronization System sync pulse indicating beginning of a 125 μsec frame.
CLK	21	Master Clock. System input clock provides basic timing for the 2952 and is synchronous to the PCM clock. The clock rate determines the number of timeslots on the transmit and receive PCM highways, ranging from 24, 32, 48 or 64 per frame.
RESET	36	Reset. (Active high input). When high, 2952 internal circuitry is reset. The minimum reset pulse must be 16 complete CLK clock cycles wide.

FUNCTIONAL DESCRIPTION

The 2952 is a highly integrated line card controller which concentrates and multiplexes all digital information that passes between a line card and the next switching or control level in a digital telecommunications system. It controls time switching functions between the individual subscriber line devices and the system backplane Time Division Multiplexed (TDM) highways. In addition, it manages the transfer of all signaling and control messages, either to an optional local microprocessor or to a central control processor. The 2952 implements all protocol control functions using the HDLC format for all information transmitted between the line card and the central processor.

EXTERNAL INTERFACE

The 2952 LCC supports interfaces for the subscriber line devices, an optional local microprocessor, and the backplane PCM and HDLC highways. Each is described briefly below.

Subscriber Line Interface

The LCC provides 8 serial, bidirectional ports for the digital transmission of voice, data, control, and signaling information to and from the subscriber. These leads, SLD0–SLD7, can be used to interface to both analog and digital line card subscribers (See Figure 3).

The Slave Clock SCL, is a fixed 512 kHz signal output used to transfer all signals between the subscriber device and the 2952. Data is received and transmitted upon the rising edge of SCL.

Data transmission direction is controlled by the Slave Direction clock, SDIR. This 8 kHz signal divides the frame transfer into transmit and receive halves referenced to the subscriber as shown in Figure 3. When SDIR is high, (RCV half-cycle), information is transmitted from the 2952 to the subscriber in four bytes consisting of voice, data, feature control, and signaling information. In the second half (XMIT-half cycle), the subscriber circuit sends four bytes of XMIT data back to the 2952.

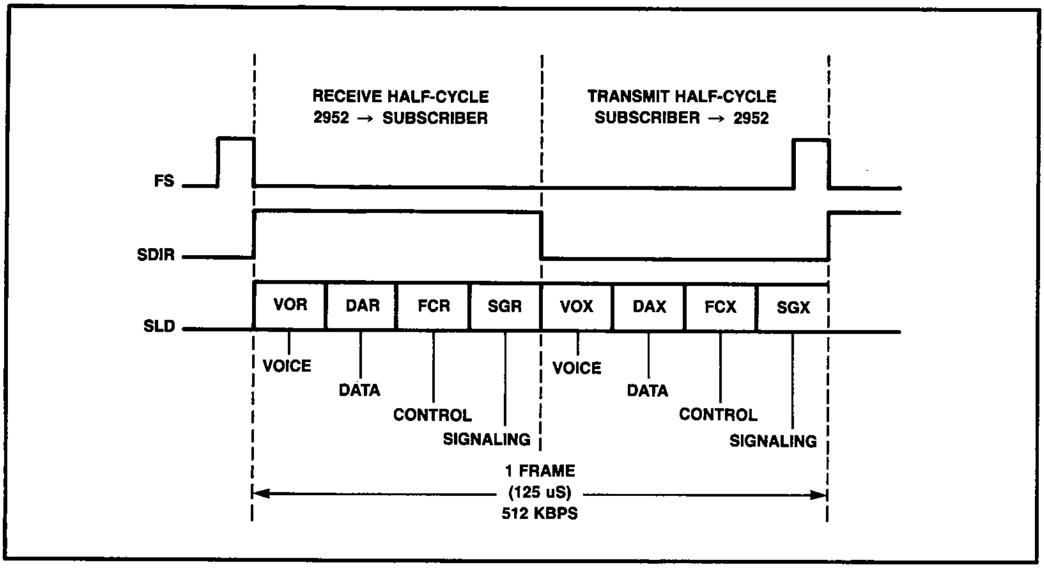


Figure 3. SLD Interface

Backplane Interface

The LCC supports dual TDM voice/data highways as well as a separate high speed serial highway for signaling and control information. This information is packetized and protected in HDLC format for transmission to a central processor.

The system clock (CLK) provides data rate transfers for both the TDM and HDLC links. The 2952 can operate in 24, 48, 32 or 64 timeslots systems. Any subscriber has access to any timeslot on either TDM highway. The 2952 allows the flexibility of programmable rising or falling edge latching of data onto the highways. Additionally, PCM highway delays can be compensated for by programming a phase shift in both transmit and receive timeslots as referenced to the frame synchronization pulse. The starting point of the bytes can be shifted up to 7 CLK clock cycles for both transmit and receive directions in half clock increments.

Microprocessor Interface

The microprocessor interface provides a communication path for a local μP and the backplane and/or slave devices. The 2952 is designed to operate with standard Intel 8-bit parallel microprocessors, such as the MCS-48, MCS-51, MCS-85, and MCS-86 families. Interrupt capability, direct-memory-access request and acknowledge signals and a full feature multiplexed address data bus are incorporated into this interface.

Alternatively, the 2952 can operate in a stand alone mode on the line card in systems using a more centralized processing architecture. In this mode, the individual line board address and initialization information is hardwired onto the microprocessor interface pins.

2952 BASE ARCHITECTURE

The 2952 can be partitioned into three functional blocks, according to the type of data transfers that each provides. The synchronous portion comprises the subscriber and PCM highway interfaces. Included in this section is also the Master Timing Unit, a CAM (Content Addressable Memory) for timeslot matching, a MODE register to configure the 2952 and for the determination of the type of HDLC data exchange, and the internal bus for a communication link between the various interfaces and registers. The PCM Interface Unit and the Subscriber Interface Unit with Last Look logic are also grouped into this segment. The Last Look logic monitors the status of signaling information received from each subscriber every frame. Any change of status is reported to the local μP or to the LCC bus control unit.

The asynchronous portion includes the local microprocessor interface and the serial HDLC signaling and control interface. The HDLC controller is compatible with ISO/CCITT recommendation X.25, and is designed for either point-to-multipoint configurations as a primary station, or in point-to-point as a secondary station. Each 2952 is accessed through

an 8-bit address, allowing up to 255 secondaries to be addressed on one HDLC serial line. The logic level of the HDLC implementation and the distribution and compilation of the data packages are handled in a separate command unit contained in this portion.

The synchronous and asynchronous portions are linked to one another by a set of buffers and a control unit for the LCC internal bus. Two 16-byte by 8-bit FIFO's are used for intermediate storage of messages. An X-FIFO, or Transmit FIFO buffers data packages for transmission to the central processor through the HDLC interface. The type of data loaded is either from the Last Look logic or from the μP in package form with direct addressing to the 2952. The Bi-FIFO, or bidirectional FIFO, is used for data exchange between the central controller (via the HDLC interface), the local microprocessor (via the μP bus), and the LCC (via the LCC bus).

MODES OF OPERATION

The 2952 may operate in either a primary or secondary command mode within a single system. When instructed as a primary station, a local microprocessor must be used to instruct the 2952 and to generate control messages for other stations. This mode is used primarily by unit or group controllers to command secondary 2952's. When in the secondary mode, the 2952 executes received HDLC commands from the group controller. Additionally, a transparent command mode may be configured in which all HDLC messages received from the backplane are passed directly to the local microprocessor. This allows a secondary 2952 to execute user defined protocol and commands.

The 2952 can operate in one of two HDLC communication modes — dedicated HDLC or interleaved HDLC. In the dedicated configuration, HDLC messages are received on DSR and are transmitted on DSX. The interleaved mode reserves up to two timeslots per frame for transmission of signaling and control messages on the PCM highways. The HDLC packets are disassembled and interleaved into programmed timeslots on either of the two highways. Alternatively, the microprocessor can communicate directly to the central controller via a direct connection, bypassing the 2952 HDLC interface completely.

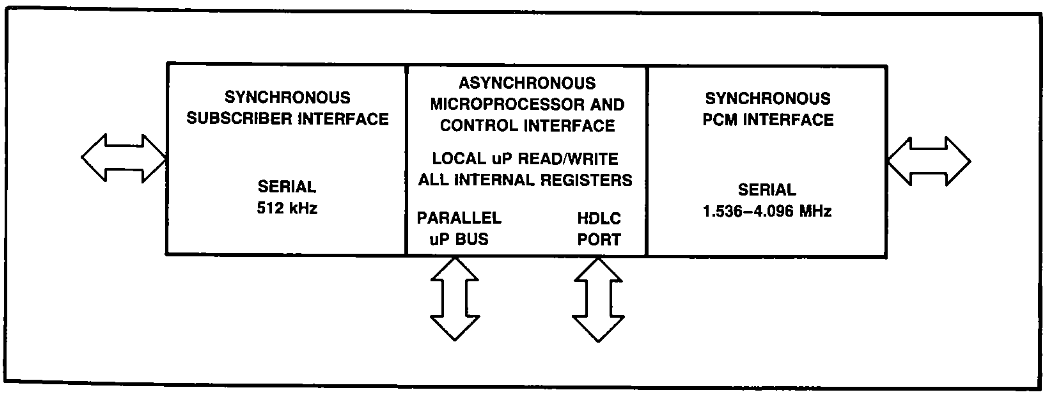


Figure 4. Architectural Diagram

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias .... −10°C to +80°C
Storage Temperature .... −65°c to 125°C
All Input and Output Voltages
with respect to GNDD .... −0.3V to +7V
Total Power Dissipation 1.5W

DC CHARACTERISTICS

(T_A = 0°C to 70°C, V_{CC} = +5V ± 5%; GNDD = 0V
Typical values are for T_A = 25°C and nominal power supply value

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
I_{IL}	Input Leakage Current	−10		+10	μA	GND ≤ V_{IN} ≤ V_{CC}
I_{OL}	Output Leakage Current	−10		+10	μA	GND ≤ V_{OUT} ≤ V_{CC}
V_{IL}	Input Low Voltage	−0.5		0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} +0.5	V		
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = +1.6 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −400 μA
I_{CC}	V_{CC} Supply Current		85	120	mA	V_{CC} = 5V
P_{D1}	Operating Power Dissipation		425		mW	

CAPACITANCE (T_A = 25°C; V_{CC} = GNDD, 0V)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
C_{IN}	Input Capacitance		5	10	pF	f_C = 1 MHz
$C_{I/O}$	Input/Output Capacitance		10	20	pF	
C_{OUT}	Output Capacitance		8	15	pF	Unmeasured pins returned to GNDD

A.C. CHARACTERISTICS

(T_A = 0°C to 70°C; V_{CC} = 5V ± 5%, GNDD = 0V)

SLD Interface Timing

Symbol	Parameter	Min	Max	Units
CLK	System Backplane Clock Frequency	1.536	4.096	MHz
	CLK Duty Cycle	45	55	%
t_{PFS}	Frame Synchronization Pulse Period	125		μS
t_{FS}	Frame Synchronization Pulse Width	60	t_{CLK}	ns
t_{dFS}	Pulse Delay to CLK	10		ns
t_{SFS}	Set-Up Time to CLK	50		ns
t_{rf}	CLKRise, Fall Times		10	ns
SCL	Slave Clock SCL Frequency	512	512	kHz
t_{dSCL}	SCL Delay Time From CLK	100	165	ns
SDIR	Slave Direction SDIR Frequency	8	8	kHz
t_{dDIR}	SDIR Delay Time to CLK	120	190	ns
t_{dSLD}	SLD Data Delay	160	300	ns
t_{DER}	Data Enable Receive	100	180	ns
t_{DDR}	Data Disable Receive	100	180	ns
t_{DEX}	Data Enable Transmit	0		ns
t_{DAX}	Data Hold Transmit	0		ns
t_{DSX}	Data Set-Up Transmit	$\frac{1}{2\ \mathrm{CLK}} + 200$		ns
t_{DSIG}	Signaling Strobe Delay	110	160	ns

A.C. CHARACTERISTICS
(T_A = 25°C, V_{CC} = GNDD = 0V)

MICROPROCESSOR INTERFACE

READ CYCLE

Symbol	Parameter	Min	Max	Units
t_{AL}	Address Set-Up to ALE	30		ns
t_{LA}	Address Hold After ALE	20		ns
t_{AA}	ALE Pulse Width	60		ns
t_{RD}	Data Delay From $\overline{RD}$		150	ns
t_{DF}	Data Float After $\overline{RD}$		25	ns
t_{RR}	$\overline{RD}$ Pulse Width	150	10^7	ns
t_{RI}	$\overline{RD}$ control interval[1]	$2 \times \frac{1}{CLK}$		ns
t_{RI}	$\overline{RD}$ control interval[2]	100		ns

WRITE CYCLE

Symbol	Parameter	Min	Max	Units
t_{DW}	Data Set-Up to $\overline{WR}$	50		ns
t_{WD}	Data Hold After $\overline{WR}$	25		ns
t_{WW}	$\overline{WR}$ Pluse Width	100		ns
t_{WI}	$\overline{WR}$ control interval[1]	$2 \times \frac{1}{CLK}$		ns
t_{WI}	$\overline{WR}$ control interval[2]	50		ns

NOTES:
1. Read or Write of BI FIFO and X FIFO.
2. Read or Write of all other registers.

DMA READ

Symbol	Parameter	Min	Max	Units
t_{DMA}	DMA Read Time		$7 \times \frac{1}{CLK}$	ns
t_{OH}	DMOR Hold Time		75	ns
t_{AR}	Address Stable before $\overline{RD}$	0		ns
t_{RD}	Data Delay from $\overline{RD}$		150	ns
t_{DH}	Data Hold after $\overline{RD}$	20		ns
t_{RA}	Address Hold after $\overline{RD}$	0		ns
t_{RR}	$\overline{RD}$ Pulse Width	150	10^4	ns

DMA WRITE

Symbol	Parameter	Min	Max	Units
t_{DMA}	DMA Write Time		$7 \times \frac{1}{CLK}$	ns
t_{IH}	DMIR Hold Time		80	ns
t_{AW}	Address Stable before $\overline{WR}$	0		ns
t_{WA}	Address Hold after $\overline{WR}$	0		ns
t_{DW}	Data Set-Up to $\overline{WR}$	30		ns
t_{WD}	Data Hold after $\overline{WR}$	25		ns
t_{WW}	$\overline{WR}$ Pulse Width	100		ns

System Backplane Timing Parameters

PCM INTERFACE — RECEIVE TIMING

Symbol	Parameter	Min	Max	Units	Test Conditions
t_{DSRR}	Receive Data Set-Up DCR = 0[1]	40		ns	60ns for Interleaved Mode
t_{DHRR}	Receive Data Hold DCR = 0[1]	10		ns	
t_{DSRF}	Receive Data Set-Up DCR = 1[2]	20		ns	
t_{DHRF}	Receive Data Hold DCR = 1[2]	40		ns	

PCM INTERFACE — TRANSMIT TIMING

Symbol	Parameter	Min	Max	Units	Test Conditions
t_{DZXR}	Data Enable DCX = 0	80	160	ns	C_L = 200pF
t_{DHXR}	Data Hold Time DCX = 0	45	160	ns	C_L = 200pF
t_{DZXF}	Data Enable DCX = 1	40	100	ns	C_L = 200pF
t_{DHXF}	Data Hold Time DCX = 1	40	100	ns	C_L = 200pF
t_{HZX}	Data Float After CLK TS	35	80	ns	C_L = 150pF
t_{SONR}	Timeslot x to enable DCX = 0	70	130	ns	C_L = 150pF
t_{SONF}	Timeslot x to enable DCX = 1	40	100	ns	C_L = 150pF
t_{SOFF}	Timeslot x to disable	40	100	ns	C_L = 150pF

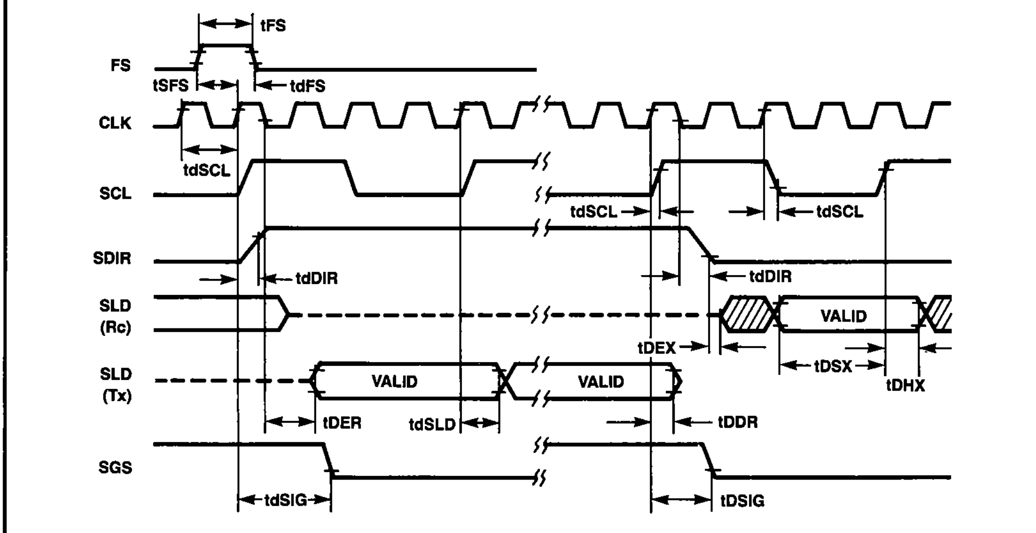
HDLC INTERFACE TIMING

Symbol	Parameter	Min	Max	Units	Test Conditions
t_{DS}	Receive Data Set Up	40		ns	
t_{DM}	Receive Data Hold	10		ns	
t_{TD}	Transmit Data Delay	40	100	ns	C_L = 200pF
t_{HZX}	Data Float on TS Exit	35	80	ns	C_L = 200pF
t_{SON}	Timeslot X to enable	40	95	ns	C_L = 150pF
t_{SOFF}	Timeslot X to enable	35	90	ns	C_L = 150pF

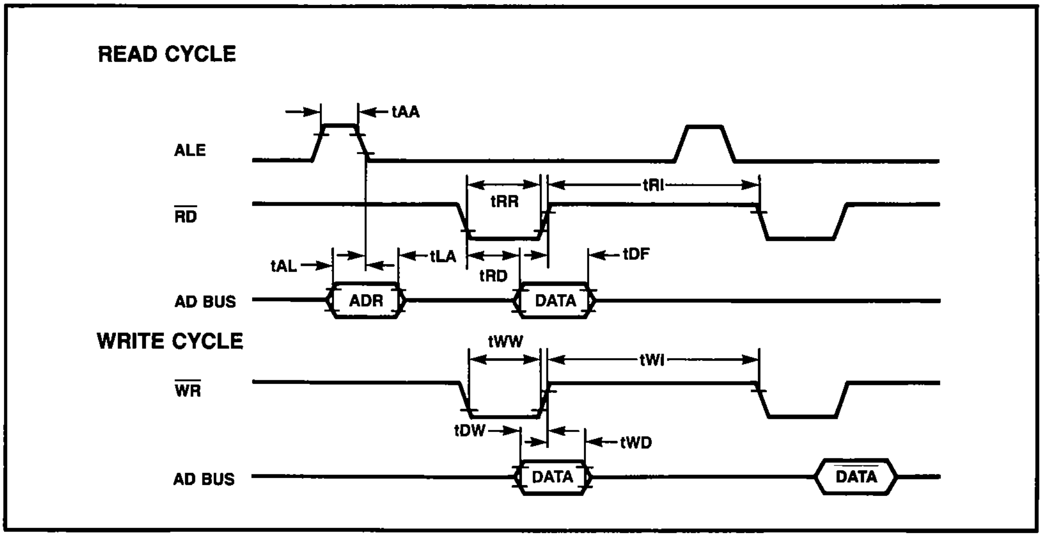
NOTE:
1. DCR = 0 data latched on rising edge of CLK.
2. DCR = 1 data latched on falling edge of CLK.

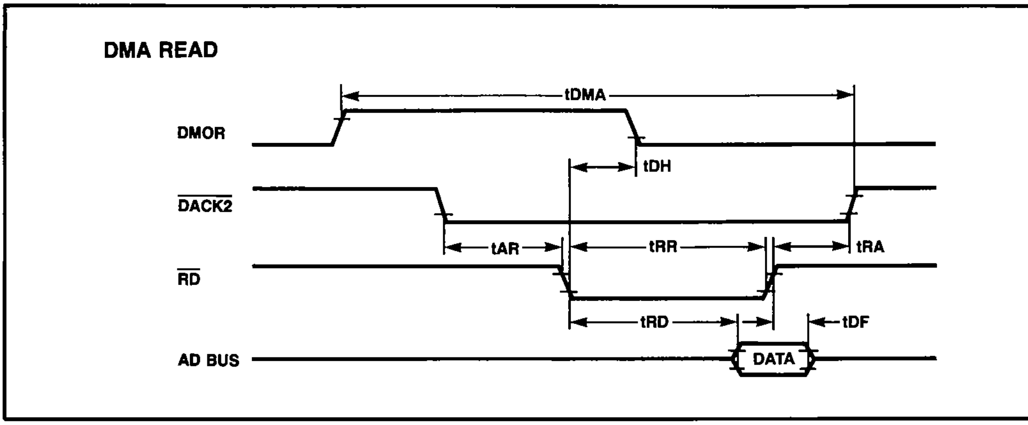
WAVEFORMS

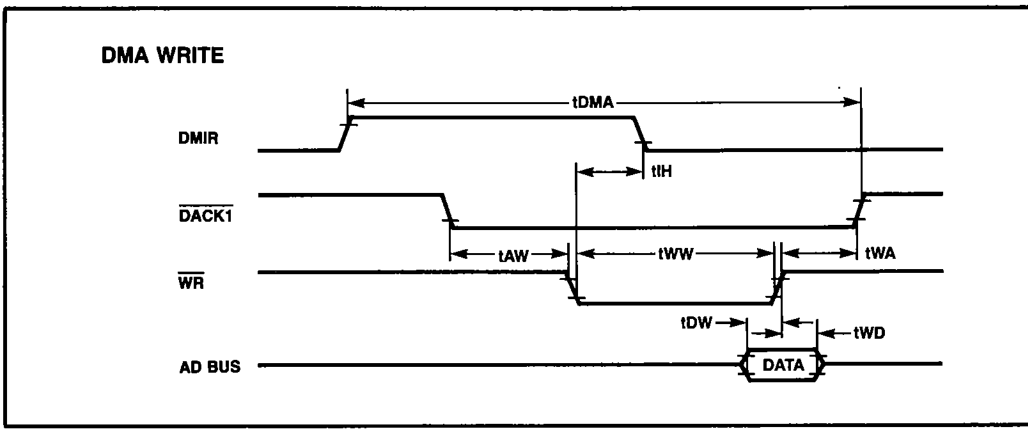
SLD Interface Timing



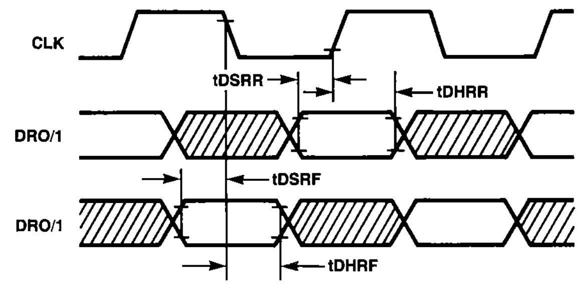
Microprocessor Interface



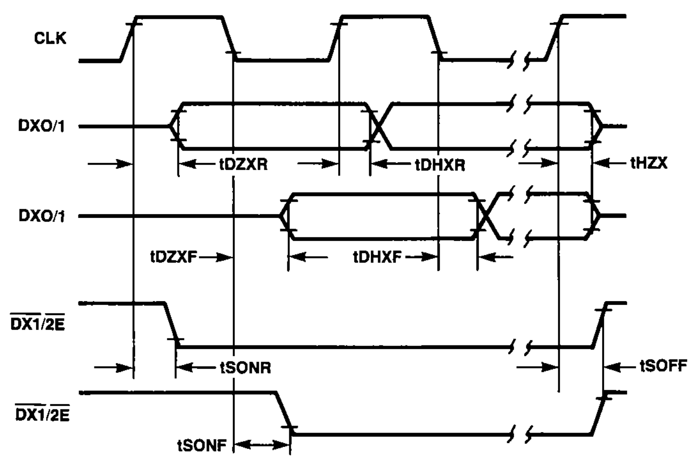

DMA READ
tDMA
DMOR
tDH
DACK2
tAR
tRR
tRA
RD
tRD
tDF
AD BUS
DATA


DMA WRITE
tDMA
DMIR
tIH
DACK1
tAW
tWW
tWA
WR
tDW
tWD
AD BUS
DATA

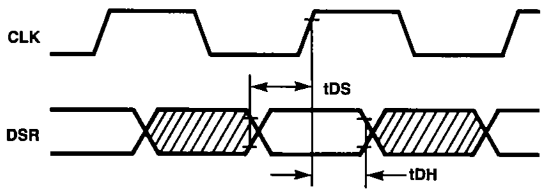
PCM INTERFACE RECEIVE TIMING



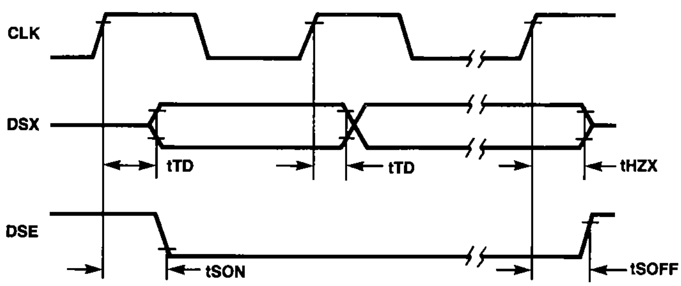
PCM INTERFACE TRANSMIT TIMING



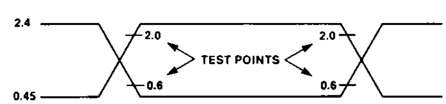
HDLC INTERFACE RECEIVE TIMING



HDLC INTERFACE TRANSMIT TIMING

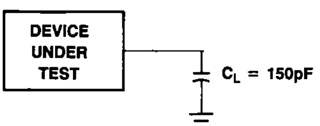


A.C. TESTING INPUT, OUTPUT WAVEFORM



A.C. TESTING INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.45V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.6V FOR A LOGIC "0".

A.C. TESTING LOAD CIRCUIT



C_L = 150pF
C_L INCLUDES JIG CAPACITANCE

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